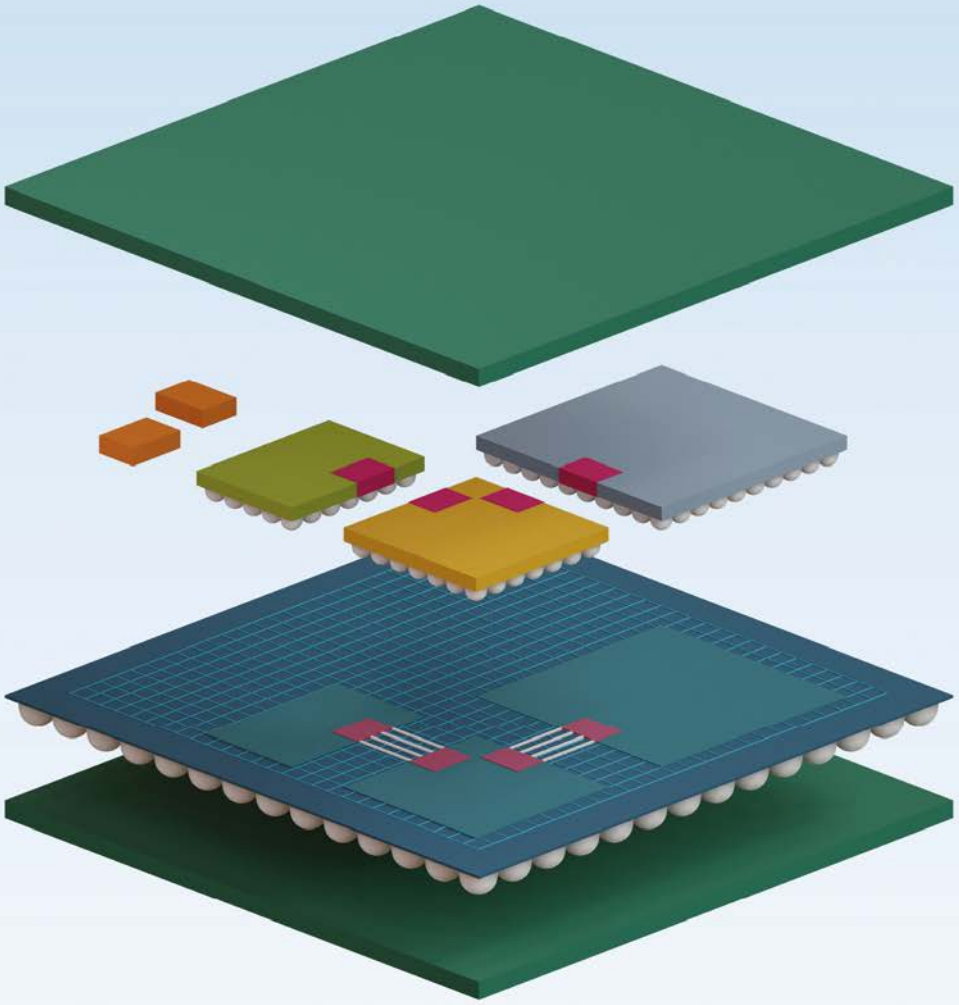

CHIP DESIGN GERMANY

AG Chiplets

CHIPLETS - DRIVERS OF INNOVATION AND SOVEREIGNTY

Chipdesign Germany
Working Group Chiplets

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1. Executive Summary

For Europe's key industries, strategic dependencies within and on the global microelectronics sector have proven particularly challenging in recent years – for example, during the COVID-19 pandemic or because of the Nexperia conflict. Resilient supply chains and technological sovereignty will therefore be critical success factors for the future in many industries. This position paper addresses decision makers in industry, politics and research.

An important building block for this is the modularization of electronics, and specifically the broader use of the chiplet approach. Chiplets are small functional units, such as accelerators, memories, or communication interfaces, that work together to realize the overall function of a larger system. They are optimized system components that are connected via die-to-die interfaces and integrated into a single package. Unlike conventional monolithic chip architectures, chiplets enable the diversification of manufacturing technologies used as well as the reuse of system designs, while offering greater potential for flexible adaptation of designs to applications, better utilization of resources, and higher supply chain resilience.

This paper sets out the strategic benefits of broader chiplet adoption, outlines the technological potential of chiplet-based approaches for European key industries and identifies action priorities as well as development needs to support the effective deployment of chiplet technology in Europe and Germany. The most important of these can be summarized in 10 points:

1. Strengthen technological sovereignty in Europe and reduce international dependencies through strategic chiplet ecosystems
2. Foster modular and resilient supply chains and strengthen regional chiplet supply chains
3. Fund advanced packaging technologies and chiplet innovation in research and development
4. Accelerate open interface standards and interoperability
5. Rapidly promote cross-industry and research collaboration as innovation partnerships
6. Support SMEs and reduce adoption barriers
7. Encourage open chiplet architectures to drive innovation
8. Support the development of reference platforms and reference designs for broad industrial adoption
9. Enable rapid joint prototyping and production capacities through pilot lines and prototyping centers with consideration of the innovative European machinery and equipment industry.
10. Invest in skills and workforce development from school and universities through workforce development

The content of this position paper incorporates not only the expertise of the contributing authors but also assessments from microelectronics experts from companies in relevant stakeholder or end-user industries. Of particular note are the representative contributions from industry associations such as AMA (Association for Sensors and Measurement), Silicon Saxony, VDA (German Association of the Automotive Industry), VDMA (Machinery and Equipment Manufacturers Association), and ZVEI (German Electro and Digital Industry Association).

2. Background

Electronics have become a key driver of economic growth, innovation, and global competitiveness. Semiconductor-based sensors, microcontrollers, memory and communication devices are essential components in practically all industrial and social sectors including defense. The electronics industry is worldwide a multi-trillion-dollar ecosystem that creates millions of jobs and drives technological advancement in sectors like telecommunication (cloud-, edge- and AI computing), automotive, autonomous systems, industrial, healthcare, energy, aerospace and finance.

Besides that, electronics are central to global value chains (GVCs) which involve the design, production, assembly and distribution of products across multiple countries. These chains are highly specialized and interdependent. In Europe, such strategic dependencies in microelectronics, especially in advanced manufacturing, skilled labor, and secure supply chains, pose especially critical challenges.

The strategic importance of electronics has therefore globally led to increased focus on supply chain resilience and technological sovereignty. Above all, the significant disruptions to the global supply of electronic components in recent years have exposed vulnerabilities to supply chains and triggered widespread economic consequences. The impact has been particularly severe in critical sectors such as automotive, industrial manufacturing, medical technology, and aerospace. Several interrelated factors have contributed to the shortage of electronic components, e.g., just-in-time manufacturing, natural disasters, pandemic disruptions, outdated architectures, and geopolitical tensions.

These factors continue to harbor the risk of long lead times, higher prices and production delays across all industries.

To overcome these challenges there are several strategies:

- Government Initiatives: The U.S. CHIPS and Science Act, the EU Chips Act as well as similar initiatives in Japan, South Korea, India, and China aim to achieve resilience, competitiveness, and innovation capacity. They are intended to boost domestic semiconductor production, to secure access to essential electronic components, and to reduce dependency on foreign suppliers.
- Reshoring and Diversification: Companies are diversifying suppliers and investing in local manufacturing to reduce dependency on single regions. Governments are incentivizing reshoring or nearshoring of strategic industrial capabilities.
- Strategic Stockpiling: Some firms and organizations are building inventories of critical components to be prepared against future disruptions.
- Regulatory / protective constraints: USA – regulation on hardware/software for connected vehicles, China – 70 new automotive standards until 2027, EU – Cyber Resilience Act

These efforts mark a shift from efficiency-driven supply chains to resilience-focused strategies with long-term implications for global trade, industrial policy, and investment decisions. However, these strategies entail significant cost increases, creating an urgent need for innovative countermeasures.

To mitigate these strategic-economic challenges in a comprehensive manner, stakeholders must adopt a multi-pronged approach:

- Invest in domestic manufacturing: Strengthening regional production capabilities and considering European equipment builders can reduce dependency and shorten response times. This requires national and

international efforts to build up capacities and capabilities
- Change in mindset: previous price advantages are often no longer available with regional production and require therefore more flexible, less price sensitive approaches and premises in the procurement of components.
- Foster collaboration: Companies, industry associations, and academia must be allowed to work together efficiently to address systemic issues like standardized platforms, interfaces, and software stacks.
- New semiconductor system design concepts: Modular architectures enable different functional blocks – like controllers and processing units – to be combined within advanced packaging, creating adaptable systems that reduce dependence on specific components and strengthen supply chain resilience. Chiplets are currently the most promising design and packaging concept of this kind.

3. Modularization of Electronics / Chiplets as an Opportunity

3.1. Chiplets Drive Future Innovation

Up to now complex electronic systems with high demands on performance and power efficiency were designed as monolithic System on Chips (SoC), i.e. the entire functionality was realized on one silicon die. As described below, due to economic constraints, the semiconductor value chain of today is globally undergoing a paradigm shift from traditional (SoC) architectures to advanced packaging technologies. Chiplets are part of this heterogeneous integration that addresses many global political and economic challenges in addition to technological advantages. There are two main drivers behind the development of chiplets which represent a continuum of variants discussed under a single term:

- High Performance Computing demands advanced technology nodes for highly regular and repetitive CPU, GPU, NPU, and memory structures. Chip die sizes get larger with yield getting close to and even beyond economically viable limits as defect densities do not decrease as easily. The defect density/yield limit can be addressed with chiplets that naturally reduce the die size towards economic viable dimensions. In single vendor scenarios these vendors break down large structures into smaller components that can be fabricated with high yield. After testing, these components are assembled into large systems on advanced chiplet interposers, without significant losses in performance and power efficiency. In such cases the yield improvement compensates the additional cost and complexity overhead associated with assembly and interposers, which today are frequently used in highly scalable data center systems.
- On the other hand, many electronic applications demand lower performances but have heterogeneous integration requirements towards various parts of their system architecture such as mixed-signal, power electronics, sensors, and control units allowing miniaturization, improved power, and cooling efficiency. These diverse requirements can best be met by integrating different semiconductor technologies into a single System in Package (SiP). Due to the lower performance requirements more cost-efficient interposers can be used. Such applications often involve smaller production volumes, making integration costly, less robust and therefore unattractive for semiconductor fabs. Heterogenous chiplet-based systems, however, offer a breakthrough: They enable the combination of higher volume chiplets with matching technology into one system. This requires a working open market with chiplets as interchangeable and cost-effective design elements. A working chiplet ecosystem supports standardized hardware and software platforms suitable for various industry sectors tailored through different chiplet configurations.

A modular chiplet-based design framework aims at mitigating the complexities associated with design scale, yield optimization, and escalating fabrication costs. This transition is on one hand driven by economic factors, including the increasing cost per transistor and the diminishing returns of Moore's Law. On the other hand, the chiplet approach also offers new perspectives in solving issues such as global supply chain unsteadiness or innovation pressure. The changeover requires advanced and comprehensive solutions that cater to a wide range of system requirements and enable efficient chip design through advanced tools and IP. To fully harness the benefits of chiplets, the industry must effectively address technical challenges of dual foundry integration, cache coherency protocols, power management strategies, and the development of a unified design methodology.

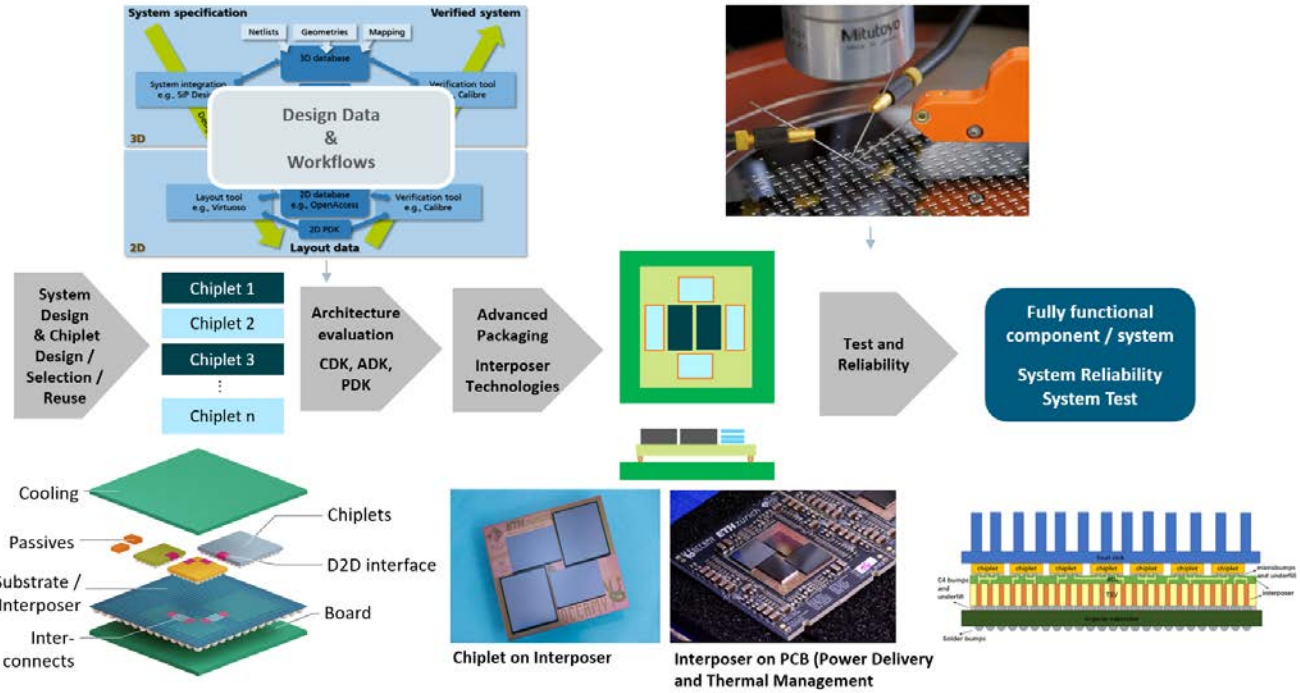

Figure 1: Simplified development flow for chiplet based systems (©Fraunhofer IIS)

From monolithic SoCs to chiplet-based systems

Chiplets are small, specialized components implementing parts of a system´s function. They work together to realize the total function of a larger system. They are optimized system components (e.g. general compute, AI accelerators, GFX engine, sensors, interfaces …) connected with die-to-die interfaces integrated in a single package to create a system. Unlike traditional designs, chiplets allow for reuse of large non differentiating parts of a system while offering more potential for customization, better use or reuse of resources, and increased supply chain resilience. This approach requires a shift from focusing only on the chip itself to planning the entire system from the start, including how chips and packaging interact over interfaces and considering additional topics from a system perspective (see Figure 2).

SoCs today pack an incredible amount of functionality onto a single silicon die. SoCs typically

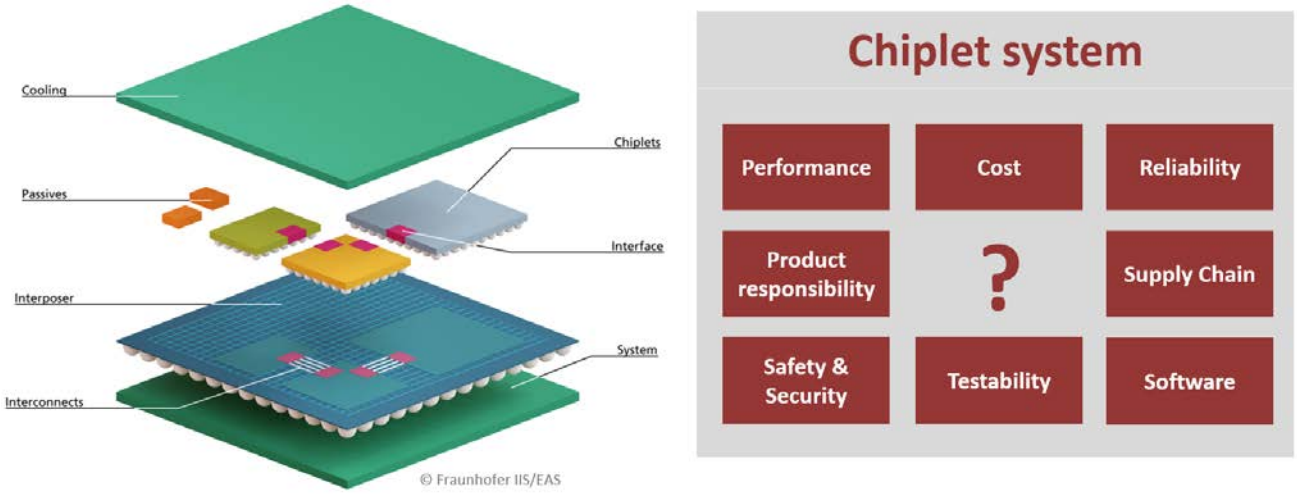

Figure 2: Topics to be addressed for chiplet-based solutions (© Fraunhofer IIS)

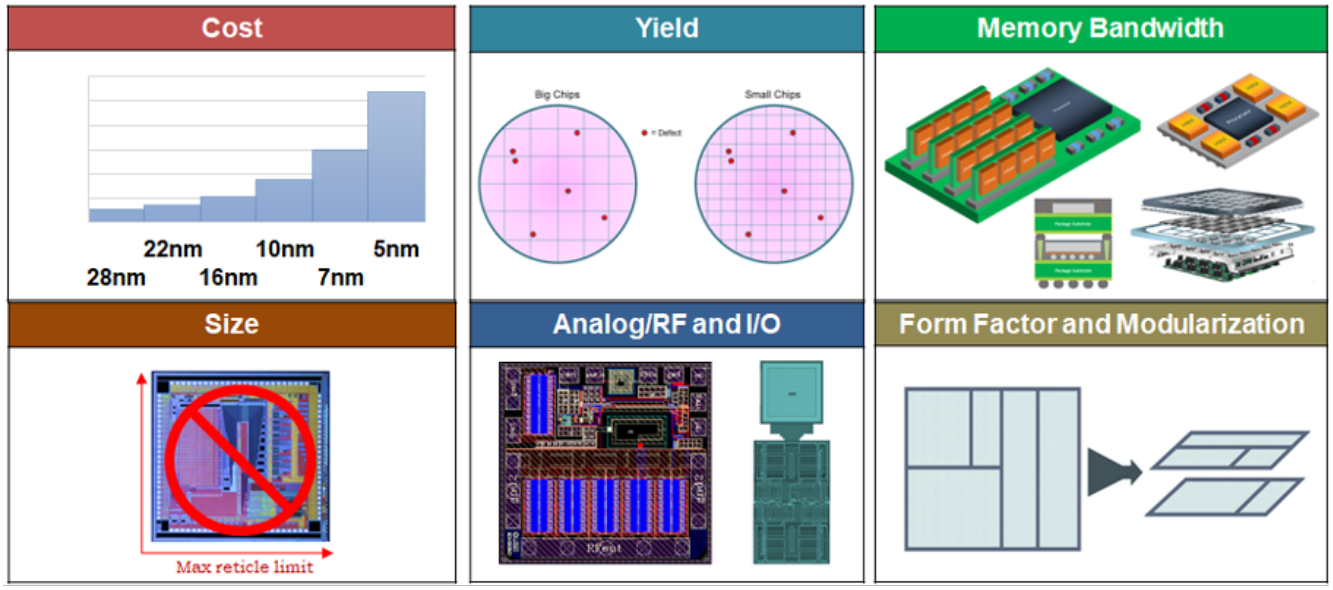

Figure 3: *Impact of Chiplet-Based Approaches on System Properties (© SIEMENS EDA)*

include a processor, digital logic, memory, and analog components, along with embedded software. Many SoCs have billions of gates and are pushing gigahertz speeds.

A major concern in SoC design is rising development costs, with estimates exceeding $500 million at the 5nm node and long development cycles requiring high volume applications to be profitable in advanced nodes.

Traditional single-die, monolithic SoCs have drawbacks, as all components are placed on the same die and node, making analog and RF design at advanced nodes very challenging. Mixed-signal integration is also difficult, as proximity of analog and digital circuits can cause problems. Separating components into different ICs requires driving signals between packages, increasing power consumption and lowering performance.

The technical advantages of chiplet-based systems, compared to traditional SoCs, can be summarized as follows:

- **Costs:** Functionalities, e.g. analog and RF, do not need to move to advanced process nodes and can help to offset the higher packaging costs.
- **Interface performance:** Decreased interconnect length and smaller pitch size enable higher interconnect bandwidth.
- **Miniaturization:** Heterogeneous integration with smaller pitch allows for saving space.
- **Power consumption:** Shorter interconnects can reduce power by avoiding big line drivers.
- **Functional integration:** Technologies e.g., photonics, PMIC or MEMS can be integrated into chiplet systems.
- **Sustainability:** Chiplet architectures improve lifecycle efficiency and reduce CO_2 footprint in Life Cycle Assesment terms through node-optimized manufacturing and modular reuse, while strengthening supply-chain resilience by reducing dependence on single advanced nodes and enabling multi-sourcing.

Thus, the chiplet approach, which focuses on consistent modularization, the use of standardized interfaces, and a holistic evaluation and optimization of the system, represents a new level of quality compared to previous concepts.

Opportunities and economic potential of chiplet-based systems

Modularization and flexibilization

Chiplets enable modular SoC design, allowing manufacturers to tailor solutions to specific customer application needs. This flexibility supports shorter innovation cycles, as designs can be quickly adapted to meet evolving requirements without starting from scratch.

Reusability

The ability to reuse proven chiplets and architectural patterns including software across different designs reduces development costs and risks in quality issues. Existing chiplets can be leveraged for multiple applications, ensuring consistency and compatibility while minimizing the need for time consuming and costly redesigns. Thus, it mitigates entry barriers for small and medium volume products.

Robustness of supply chains

Chiplets foster a B2B ecosystem, where components can be sourced from multiple vendors rather than relying on a single supplier for entire chip designs. This diversification enhances supply chain resilience, reduces dependency risks, and mitigates disruptions. Additionally, chiplets open new business models, such as licensing and selling individual components, further diversifying revenue streams.

Obstacles

Despite their potential, chiplets face several challenges that must be addressed to demonstrate their full benefits:

Standardization and B2B ecosystem development: A robust ecosystem with clearly defined reference architectures and compliance standards is essential for a wider chiplet adoption. Without standardization, interoperability between chiplets from different vendors becomes a significant hurdle.

Integration complexity: Package-level integration of chiplets requires advanced technologies and expertise, which may increase complexity and initial development costs. Although several point tools are available today to design a chiplet-based system, it's up to each design team to develop their own methodologies to integrate the flow. This makes designing a chiplet-based system today quite a challenge.

Performance trade-offs: While modularity offers flexibility, it may introduce latency or power inefficiencies compared to monolithic designs. These trade-offs must be carefully managed, especially for high-performance automotive applications.

Modularity of the chiplet interfaces: The modularity requirements relate to Design-for-Test and Design-for-Manufacturing, as well as to the die-2-die interface regarding standards and protocols, JTAG, Reset, clock, I3C, the control of the power-on sequence, and the boot strap of the entire system.

3.2. Current Situation – Challenges and Gaps

The semiconductor industry is shifting towards modular chiplet designs to meet growing complexity and cost pressures. This approach requires advanced packaging and a new design mindset – focusing on system-level integration rather than individual chips. While promising, it also demands progress in design tools, standards, and ecosystem collaboration. The current landscape of chiplet design, manufacturing including equipment, and integration can be explored through several key areas:

Heterointegration and advanced packaging

Package-level integration facilitates the adoption of heterogeneous chiplet dies, each developed with an optimized process tailored to its specific function. This modular approach enhances flexibility, scalability, and reuse, while mitigating yield issues associated with larger die sizes. Advanced packaging techniques, such as substrate technologies (IC, ABF, glass), TSVs, and micro bumps, play a critical role in connecting chiplets to achieve desired functionality and performance at economically viable costs.

Due to the variety of requirements, especially in use cases with smaller production volumes (industrial, medical, aeronautics, and space), advanced packaging techniques and chiplet solutions will always be supported by classical heterogeneous integration approaches, finding the optimal trade-off between initial efforts and productions costs.

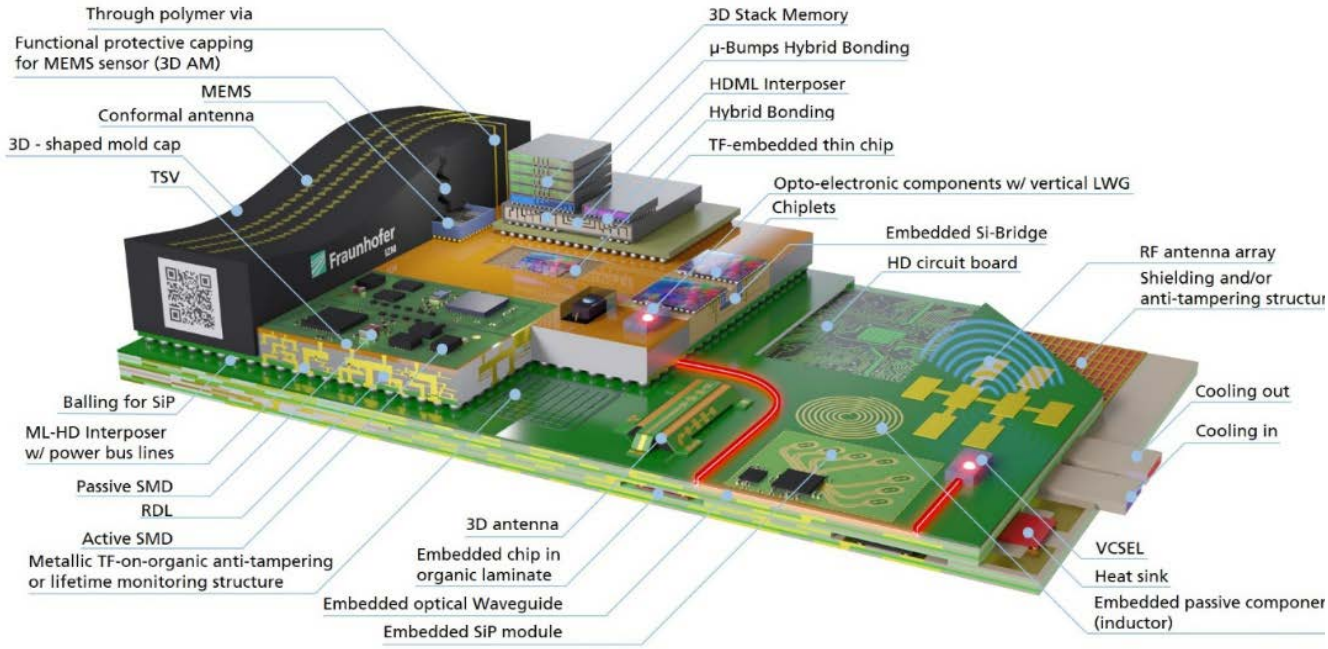

Figure 4: *Capabilities of Advanced Packaging / System integration (© Fraunhofer IZM)*

Single vendor chiplet solutions

Commercially available solutions are currently dominated by closed vendor-specific solutions utilizing some of the chiplet benefits for the required system. While this approach ensures compatibility and optimization within a single vendor's ecosystem, it limits interoperability and broader adoption across the industry. Examples for vendor specific solutions are AI training solutions from Nvidia and AMD leveraging chiplet base approach to increase the compute die size beyond the maximum die size limits or Intel which is using a chiplet-based architecture for the last couple of generations for CPUs for PC and servers to mix different technologies for different functions as well as increasing the portfolio by using chiplets with different capabilities.

Design tools and flows for heterogenous integration, 2.5 and 3D

The integration of heterogeneous chiplets demands sophisticated design tools and workflows to manage the complexity of package-level integration. These tools must address challenges such as thermal management, signal integrity, and power delivery, ensuring seamless operation of the integrated system.

The integration of chiplets has revolutionized the way engineers design complex devices. By assembling various third-party IPs as chiplets that are integrated into advanced packages, engineers can rapidly and cost-effectively create sophisticated System in Packages. However, current design tools and methodologies were primarily developed for monolithic devices, focusing on one device level at a time. As a result, they are not sufficient to fully harness the optimization potential of a chiplet-based approach. To address this issue, 2.5D/3D IC design using chiplets represents an inflection point that requires a system-centric approach from early planning through final sign-off.

Current methods deployed are commonly known as device technology co-optimization (DTCO), which are focused on single monolithic die packages. This needs to shift to what is considered as system technology co-optimization (STCO), which enables co-design and optimization across the entire package assembly, from silicon dies / chiplets to the PCB motherboard.

Heterogeneous integration brings together multiple semiconductor components into one advanced system. To make this possible, experts move through a structured process that begins

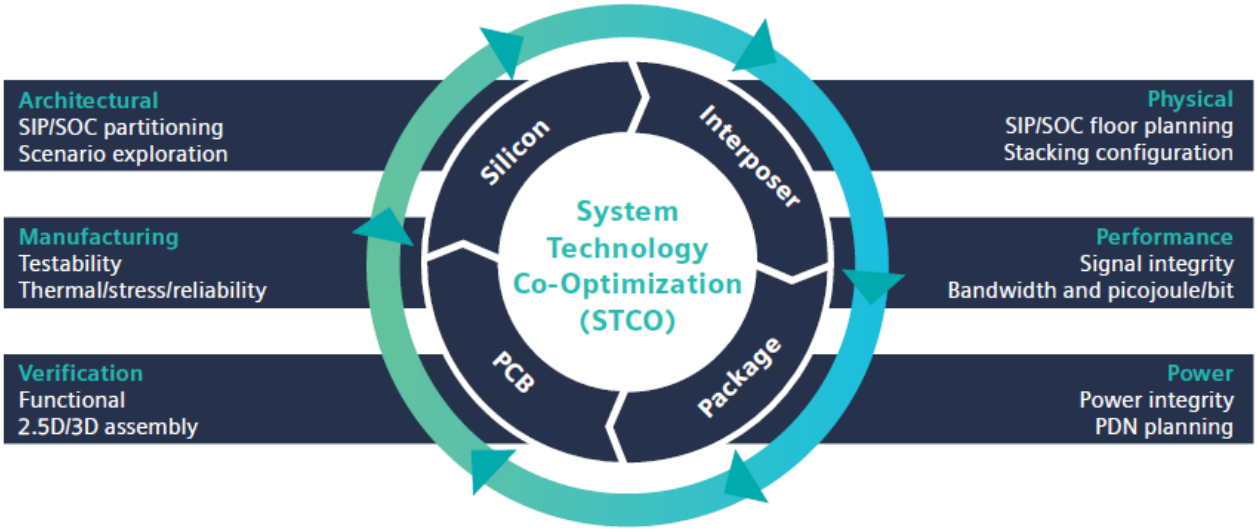

Figure 5: *STCO enables co-design and optimization across the entire package assembly, from the silicon die to the PCB motherboard (© SIEMENS EDA)*

with collecting all essential design information and creating a detailed 3D digital model. This model supports early decisions about how different chips should be arranged and connected. The team then refines the overall layout to ensure efficiency, reliability, robustness, and testability while coordinating closely on mechanical aspects like stability and heat management. Interfaces between components are planned carefully, and early computer-based analyses help optimize performance, energy use, size, and cost. Before final production, the complete system is checked thoroughly to identify issues early, and once the design is validated, it is prepared for manufacturing tools. The process concludes with final quality checks to ensure the product can be produced reliably on a scale.

Chiplet initiatives

The European Union's Chips Act, the U.S. CHIPS and Science Act, Japanese's ASRA, Europe's CHASSIS, Semiconductor Coalition Europe and Chiplet Application Hub chiplet initiatives, Korea's BOS-CarOEM chiplet platform, and China's Chipuller patent portfolio extension are examples of policy responses aimed at securing access to essential electronic components and reducing dependency on foreign suppliers.

Industry initiatives (e.g., ASRA) and efforts by research organizations (e.g., imec, Fraunhofer) are actively exploring the potential of chiplets, with collaboration between semiconductor manufacturers, research institutions, and OEMs driving innovation. In addition to developing a common understanding of the need for action these initiatives aim to establish proof-of-concept designs, validate chiplet-based systems, demonstrate their viability for application domains like automotive and other applications, and create a methodology for early evaluation of chiplet systems.

Japan's ASRA, a consortium of major automotive and semiconductor companies, is advancing chiplet-based development to increase flexibility, performance, and manufacturability for future vehicles. Imec collaborates closely with ASRA through its Automotive Chiplet Program (ACP), which unites nearly 20 international partners to define shared automotive chiplet architectures, promote interoperability, and publish joint specifications by 2026. Research Fab Microelectronics Germany (FMD) complement these efforts in Europe by driving advanced packaging research, heterogeneous integration, and chiplet-ready manufacturing through initiatives like the Chiplet Center of Excellence (CCoE) and the APECS pilot line established under the EU Chips Act. This work focuses on providing innovative integration technologies accompanied by a systematic approach to enable an early

estimation of performance, cost and reliability and innovation of chiplet systems. The goal is to provide a flexible tool set and validated date to enable robust, scalable chiplet solutions and high-density packaging technologies essential for industrial and automotive applications.

Within the project CHASSIS, funded in the Chips JU framework, leading innovators from Europe's mobility, semiconductor and software industries collaborate with prominent research institutions to create scalable, high-performance chiplet platforms for software-defined vehicles (SDVs). With the chiplet approach limitations of traditional monolithic SoCs will be overcome and development, integration and deployment of automotive electronics will be redefined.

Standardization activities

Standardization is the cornerstone of building a robust chiplet ecosystem. Early chiplet systems relied on custom die-to-die interfaces, non-uniform packaging schemes, and limited tooling support, which led to fragmented development environments, high integration costs, and constrained supplier networks. By defining common physical interfaces, protocol behaviors, and system-level integration rules, standardization eliminates these inefficiencies. It ensures that chiplets from different vendors, design teams, or process nodes can reliably interoperate within a single package. Furthermore, shared compliance and validation frameworks enable common design and verification methodologies, lowering barriers for new participants and accelerating time-to-market for complex systems.

The Universal Chiplet Interconnect Express (UCIe) standard provides a comprehensive framework to address interoperability and integration challenges inherent to chiplet-based systems. UCIe employs layered architecture encompassing protocol, adapter, and physical layers, enabling multi-protocol support for diverse performance envelopes and application domains. UCIe's flexibility has enabled advanced packaging configurations across sectors such as automotive, data centers, AI accelerators, and edge computing platforms.

Among others, as an alternative approach for die-to-die interface standardization, Bunch of Wires (BoW) is being developed by the Open Compute Project (OCP). OCP's Chiplet Design Exchange (CDX) framework focuses on standard metadata and machine-readable descriptions to streamline IP exchange and tool interoperability. DARPA's CHIPS (Common Heterogeneous Integration and IP Reuse Strategies) program laid the foundation for modularity and reuse across process nodes and vendors, influencing early standardization efforts. Intel's Advanced Interface Bus (AIB) demonstrated high-speed intra-package communication and paved the way for UCIe. Additionally, the IEEE Heterogeneous Integration Roadmap (HIR) provides long-term targets for packaging and integration technologies, including chiplet adoption and co-packaged optics.

In safety-critical domains like automotive, initiatives align chiplet design practices with ISO 26262 standards, ensuring functional safety compliance.

Standards that are not primarily geared toward HPC applications but rather address the needs of the mid-range and low performance segments and support the mixture of different semiconductor technologies, remain underrepresented in current standardization efforts. Yet it is precisely these standards that are of particular importance to key European industries.

3.3. Requirements for a Multi-vendor Chiplet Ecosystem

Chiplet-based systems may never become "mainstream" and step outside the IDM world unless they can be designed and produced in a cost-effective way, with sufficient turnaround time to meet market windows. This will be possible only with a robust and well-defined open supply chain ecosystem, including semiconductor design companies, EDA vendors, IP suppliers, foundries, outsourced semiconductor

assembly and test (OSAT) providers, and machine manufacturers. In principle, approaches at the wafer and package levels need to be more closely integrated to realise the benefits of advanced 3D packaging.

Foundries need to continue establishing design rules, create models and libraries, and provide process design kits (PDKs) and reference flows for chiplet-based systems. However, they might need to extend their role by starting to provide assembly design kits (ADKs) that extend coverage beyond 2.5D/3D integration and into 3D packaging. Other components of an ADK would be system-level libraries and models as well as compliance kits to electrically validate chiplet-to-chiplet interfaces.

New capabilities are needed in such areas as partitioning and functional splitting, system-level exploration, 3D floor planning, implementation, extraction/analysis, test, and IC/package co-design forward to a system-co-design. For optimal, timely, cost-effective design, a 3D-IC flow will support unified design intent, abstraction, and convergence with physical and manufacturing data. The open chiplet ecosystem needs to emerge, with design kits and reference flows.

However, there are other application-specific requirements that must be considered. In Table 1 table key challenges for important European industries are shown.

The technological development toward chiplet-based systems is mainly driven by applications in data centres, consumer products, autonomous system, and currently also in the automotive industry. Therefore, these industries will be discussed in more detail. Applications in industrial automation, medical technology, aerospace, and the defence sector can benefit in the medium term from technological advances (e.g., miniaturization, increased performance in RF-applications), defined and proven standards, and the establishment of a multi-vendor chiplet ecosystem.

Consumer and datacenter

Based on the proximity of chiplets and the very high number of connections between chiplets, the chiplet technology allows for very low power and low latency highspeed interconnects between chiplets. This enables to break up (disaggregate) monolithic chips in multiple chiplets.

This new design opportunity can be used to create a “virtual” chip created of multiple chiplets allowing to increase overall chip size, reuse

Automotive	Industrial	Medical	Military / Aerospace
▪ Complex architecture ▪ Complex supply chains ▪ Low priority in semiconductor allocation ▪ Heavy dependency on electronic components ▪ Shift to electric / autonomous vehicles ▪ Automotive tech-node manufacturer capacity shift to China ▪ Advanced tech- node competition with non-automotive sectors	▪ Component diversity ▪ Long product lifecycles ▪ Global dependencies ▪ Low volumes of OEMs cause high cost for ASICs ▪ Low attention / less attractive for semiconductor fabs	▪ Regulatory ▪ constraints ▪ Precision and reliability ▪ Highly specialized electronic components ▪ Limited suppliers and specialized manufacturers ▪ Quality control and component selection costs	▪ Stringent certification ▪ Long development cycles ▪ Security, reliability and sovereignty ▪ Advanced-node and edge-AI reliability / radiation hardness

Table 1: Key Challenges for important European industries

individual chiplets for multiple chips and use different optimized technologies for the chiplets.

A couple of concrete use cases in the datacenter and consumer sector:

- High performance AI trainings accelerators using chiplet methodology to increase the maximum chip size beyond the physical limit by combining multiple identical chiplets to one chip, creating an overall more powerful chip.
- Intel is using the chiplet concept in the consumer CPU area to create multiple products with different combinations of chiplets to address different markets without increasing R&D effort. An additional advantage of this concept is the opportunity to use optimized technologies for different chiplets. The computation intensive part of the overall product will benefit from the latest (but expensive) technology, but the external interface part can be done on a more mature technology with lower costs.

The key drivers for innovation around advanced packaging are AI accelerator systems. The major bottleneck for performance improvements is the interface between compute clusters and large memories. The packaging innovation of combining DRAMs with large capacity (HBM memory) and AI accelerator chips in an advanced package, which allows a very high number of connections between the compute chip and the memory chip, has been instrumental to increase the bandwidth between the two chips while keeping power consumption and latency low. This is not exactly a chiplet package but a major technology enabler and volume driver and precursor for the chiplet industry and currently the only system, in which the package is built with standardized components (HBM memories) from multiple vendors.

Automotive

The automotive industry has requirements for semiconductor solutions, including high reliability, safety, security, scalability, and performance in harsh environments. To enable the adoption of chiplet-based systems in this domain, a robust multi-vendor chiplet ecosystem must be established. This ecosystem should address technical, operational, and business challenges while fostering collaboration across the value chain. Below are the key requirements for such an ecosystem, specifically tailored to automotive applications:

1. **Availability of reference system architecture**
   A foundational requirement for a multi-vendor chiplet ecosystem is the availability of a well-defined open reference system architecture. This architecture serves as a blueprint, allowing multiple chiplet suppliers to design and develop components that seamlessly fit into the system. It ensures interoperability and provides a common framework for innovation, enabling OEMs and Tier 1 suppliers to mix and match chiplets from different vendors without compatibility issues.
2. **Virtual prototype for early development**
   To accelerate chiplet adoption, a virtual prototype of the reference system architecture is essential. This prototype allows chiplet suppliers to begin development early, ensuring their components align with the architecture. Additionally, it enables automotive OEMs to start software development in parallel, reducing overall development cycles and ensuring that software integration is ready when hardware samples become available.
3. **Availability of golden dies**
   Golden dies serve as reference chiplets for interoperability testing and are essential for validating the integration of chiplets from multiple vendors. These dies act as benchmarks, ensuring that IPs from various suppliers can communicate effectively and meet performance requirements. Golden dies also help identify and resolve challenges of integration early in the development process.
4. **Openness of the chiplet architecture**
   An open chiplet-based architecture is vital to prevent vendor lock-in and reduce costs associated with proprietary solutions. By

enabling competition among chiplet suppliers, openness fosters innovation and ensures that OEMs have access to a diverse range of components optimized for performance, cost, and scalability. This openness also encourages collaboration across the ecosystem, driving advancements in chiplet technology.

5. **Responsible entity for chiplet integration**
   Unlike hyperscalers, which can bear the risk of integrating chiplets themselves, automotive OEMs require suppliers to take responsibility for chiplet integration. A dedicated entity such as a chiplet system integrator has to be responsible for the functional integration and verification of chiplets from different vendors. This entity ensures that the final product meets automotive-grade requirements, including safety, reliability, and performance.
6. **Package quality and reliability data**
   The automotive industry demands robust solutions capable of withstanding harsh environmental conditions, such as extreme temperatures and vibrations. To meet these requirements, the chiplet ecosystem must provide package quality and reliability data points. These data points guarantee the durability and robustness of the final solution, ensuring long-term reliability in automotive applications.
7. **Fitting software ecosystem**
   A software ecosystem tailored to chiplet-based systems is crucial for seamless integration and operation. This includes tools for software development, debugging, and validation, as well as frameworks that support mixed-criticality applications. A well-defined software ecosystem ensures compatibility across chiplets and accelerates the deployment of automotive-grade solutions.
8. **Early samples for technology readiness**
   Early samples of chiplet-based systems are necessary to demonstrate the readiness of technology iterations. These samples allow OEMs and Tier 1 suppliers to validate hardware functionality and begin software integration ahead of full-scale production. Early access to prototypes ensures that any issues are identified and resolved before mass deployment.

The establishment of a multi-vendor chiplet ecosystem tailored to the automotive industry requires collaboration across semiconductor manufacturers, system integrators, and OEMs. The full potential of chiplet-based systems can be unlocked by addressing key requirements such as open reference architectures, interoperability standards, and robust integration processes. This approach not only accelerates innovation but also ensures that automotive-grade solutions meet the industry's stringent demands for safety, reliability, and scalability.

Applications in industrial automation, medical technology, and aerospace

These applications are characterized by smaller production volumes (usually significantly less than 100,000 chips per year) and the associated high degree of diversification. Nevertheless, advances in advanced packaging and chiplet technologies can also be directly applied in these applications:

- For RF packages, chip-scale packaging and interposer technologies offer the possibility of realizing miniaturized multi-chip packages with low inductive losses. This means that industrially scalable packaging technologies are becoming available for even higher frequencies, replacing the previous mostly mechanical-manual manufacturing processes.
- About the thermal management of chiplet packages, bidirectional innovation options are available for power modules and packages for power electronics.
- Sensor systems already combine a wide variety of chip technologies for signal conversion, further processing, and power supply. There is potential for the immediate use of chiplet innovations in terms of uniform interfaces, form factors, and reliability. This applies to the future field of photonic packaging.

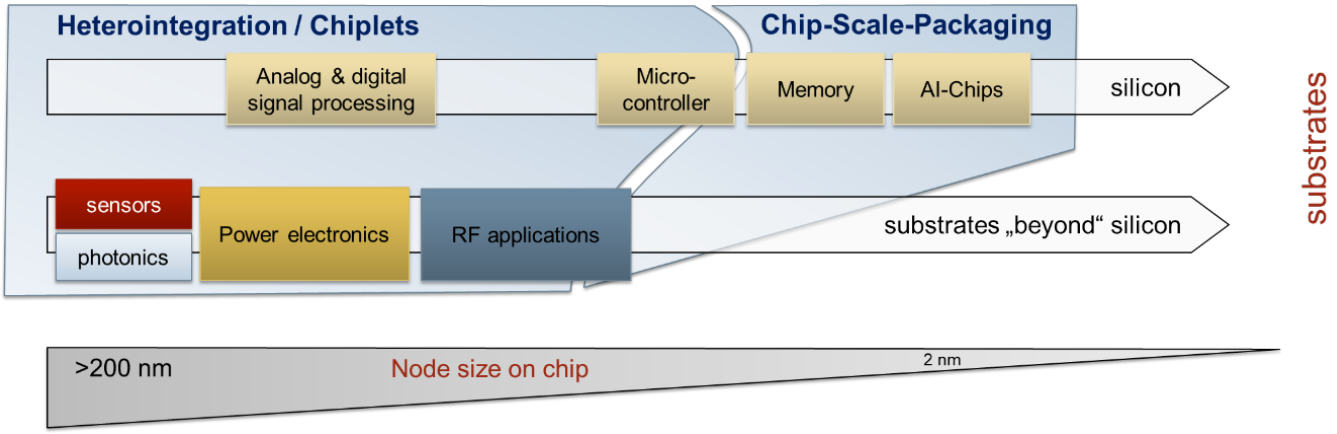

Figure 6: *Packaging innovations supporting applications with smaller production volumes (© Hahn-Schickard-Gesellschaft)*

Technology trends and cross-industry requirements from the perspective of sensor technology are presented in the “Sensor Trends 2030” study by the AMA Association.

Requirements traditionally associated with the automotive sector, including high reliability, safety, scalability and robust performance under challenging environmental conditions, are equally relevant for the application areas addressed here, including mechanical and plant engineering and autonomous systems (physical AI). This offers the opportunity to draw on the experience gained from implementing chiplet-based systems and to develop cross-industry platforms.

4. Needs for Action and Development Requirements

Based on a broad survey of representatives from industry associations in German key industries and the contribution of representative industry associations such as AMA, Silicon Saxony, VDA, VDMA, and ZVEI, it can be concluded that chiplets could be a potential strategic lever for innovation, variety, and flexibility in electronic products made in Europe. This applies to products with medium or small quantities, a wide range of functional variants or more complex chip structures. Chiplets make it possible to use technologies and components from different manufacturers in the development phase of electronic systems and integrate them into a powerful system. These combination options allow a wide range of products with different performance and functionality requirements to be covered efficiently. System developers can adapt designs to new requirements relatively quickly.

However, the most important strategic advantage over previous architectures is that the increased use of chiplets makes it possible to break up the existing supply chains, which have become very vulnerable. In recent years, numerous industries have experienced painful dependencies, especially on Asian and specifically Chinese electronics manufacturers. The modular approach raises hopes that Europe and Germany will once again be in the position to play a significantly greater role in this context and to achieve more sovereignty.

The key to the success of chiplet-based solutions will depend on whether the anticipated innovation potential can be realized and whether the requirements for performance, miniaturization, and reliability can be met in mass production at reasonable cost.

Establishment of a viable open multi-vendor chiplet ecosystem

The basis for greater use of chiplet solutions by German and European companies is a general rethinking of business models and supplier relationships. Whereas the focus has often been on performance evaluation and maximizing cost savings, the diversification of supply chains and the development of additional added value must now take on far greater importance. Geopolitical risks are undeniably becoming an increasingly relevant economic risk that must be addressed. Chiplets can reduce dependencies in a supply chain on one or only a few semiconductor manufacturers and strengthen technological sovereignty, as they can be sourced from different suppliers. Flexible production and test concepts and sources of supply, design variety, and reusability also help to respond more quickly to the demands of increasingly volatile markets and further increase the resilience of companies.

In addition, companies and research institutions focusing on transfer in Germany and Europe should definitely join forces to develop unique European selling points and competencies. This great opportunity can only be exploited in international competition if ecosystems and innovation partnerships are established quickly.

Build Technological Sovereignty

"Strengthen Europe's semiconductor sovereignty through strategic chiplet ecosystems."

"Reduce foreign dependencies by empowering regional chiplet supply chains."

Foster Resilient Supply Chains

"Turn modular design into modular supply chains – flexible, diverse, resilient."

"Chiplets as Europe's lever to break vulnerability in global electronics."

Despite all advantages that the use of chiplet technologies brings in an overarching context, it is of course also necessary to consider the cost factors for each individual company along the electronics manufacturing chain and in productization, as cost sensitivity is very pronounced in

many industries. When it comes to high volumes, chiplets tend to be at a disadvantage compared to monolithic chip designs. However, an economic comprehensive analysis could be much more positive for specific high-volume applications and for medium and low batch sizes, which are typical for traditional European industries. It is imperative that such an analysis be conducted openly and actively within the German and European ecosystem, taking competitive advantages into account.

Foster cooperation between universities, RTOs and industry

One important aspect for success and competitiveness in Germany and Europe is to leverage the potential of cooperation. Joint innovation between companies and research institutions must be set up in a way that innovative results from research can be rapidly transferred to industrial application and production ramp-up. Especially for SMEs, cooperations with applied research are crucial, as these companies will be at a significant disadvantage in the development and use of new technologies without research partners.

Support SMEs & Reduce Adoption Barriers

"Empower SMEs with shared platforms, reference designs, and low cost access."

"Lower entry barriers to make chiplets a tool for all European industries."

Support the development of reference platforms and reference designs

Enable Rapid Prototyping & Production Capacity

"Provide pilot lines and prototyping hubs to turn ideas into chips fast."

"Make Europe the place where semiconductor innovation becomes reality."

It is essential that the work focuses on the most important requirements of the respective core industries. Generic open reference platforms, developed and driven by industry, are required to enable the rapid adoption of chiplet-based approaches. These must provide architectural variants, a sufficient set of characterized basic elements, model libraries, standardized workflows, reference implementations (golden dies or devices), and methods for verifying standard compliance. Furthermore, these platforms should ideally be based on a set of uniform, flexibly expandable elements and should be easily adaptable to industry-specific requirements. In addition to the hardware elements, software must also be considered. An essential component of the platform must therefore also be a uniform, ideally cross-industry software stack.

Approaches for joint prototype development must be developed so that the costs of feasibility studies can be shared between partners. This reduces effort and risks and offers the opportunity to document the findings and data obtained in a comprehensible manner and make them available within the ecosystem.

Standardization

The aim of standardization must be to quickly develop a common understanding of practical options for implementing chiplet-based systems.

Accelerate Standards & Interoperability

"Make standards the backbone of Europe's chiplet economy."

"Unify interfaces to unlock a multi-vendor chiplet marketplace."

Encourage Open Architectures

"Open chiplet architectures prevent lock in and boost competition."

"Openness drives innovation – mandate it, support it, scale it."

A multi-stage approach is desirable, in which suitable guidelines are developed based on best practice examples and the implementation of reference architectures, which could represent a preliminary stage or at least a temporary substitute for a standard. Standardization must focus on compatibility with the requirements of key European industries. Since chiplet-based systems integrate multiple chips, standardization should focus on open interfaces. This includes not only electrical properties but also geometric aspects and material compatibility.

The joint development of concepts and architectures, as well as the exchange and sharing of best practices, reference architectures and guidelines in the chiplet ecosystem, must be in line with legal regulations. Therefore, antitrust regulations must be adopted to make this possible.

Framework conditions and funding

The political and legal framework conditions must be optimized to promote the introduction and widespread use of chiplet technologies. This includes general measures for the electronics industry in Europe, such as ensuring the availability of materials for microelectronics production at the European level or strengthening and streamlining national administrations for the further expansion of production capacities. Since a stronger focus on chiplet technologies can bring competitive advantages for domestic products and increase resilience, a correspondingly oriented location policy is essential. This includes, among other things, ensuring that funding policy continues to promote and clearly prioritize the development of chiplets and advanced packaging, as these areas are currently still “underrepresented” in Europe. Furthermore, the broader structural framework, including taxation and duties, bureaucracy, planning and approval procedures, and infrastructure, must be designed in a way that enables technological advancements to quickly strengthen competitiveness and technological sovereignty.

The EU Chips Act, which aims to promote the continent's technological sovereignty, is an important first step. However, further national measures are needed to bring about a lasting paradigm shift in the economy. These include increasing funding for the electronics industry with a clear focus on innovation and European resilience to international influences, as well as clearly taking economic needs into account from an overarching perspective (no promotion of individual corporate interests). Specific public and private financing approaches could also be interesting here to support focused technological development and the creation of unique European selling points. The funding criteria could include that funded innovations must stand out from the market and be competitive in the long term.

Fund Advanced Packaging & Chiplet Innovation

“Invest in advanced packaging – where the next generation of semiconductor value is created.”

“Support chiplet R&D to secure Europe’s competitive edge.”

Enable Industrial Collaboration

“Promote cross industry and research partnerships to turn innovation into impact.”

“Break silos – build ecosystems.”

The success of chiplet technologies across company boundaries depends fundamentally on the availability of compatible and widely adopted interface standards. Strengthening standardization therefore constitutes a key strategic priority. Policymakers should reinforce the framework conditions for the development, establishment, and international alignment of such standards at both the European and global level. Standards must be made available in a timely and cost-effective manner to a broad base of companies, including small and medium-sized enterprises in Europe. Targeted

policy instruments should support the definition, adoption, and practical implementation of standards, with a particular focus on SMEs. In addition, measures that facilitate access to chiplet integration technologies for smaller companies are recommended. Continued and coordinated support for established industrial and research consortia within the chiplet ecosystem should be an integral part of this approach.

Availability of skilled labor

The shortage of skilled workers is already a massive problem in the electronics industry in general and is even more acute for advanced packaging experts in Europe, where this topic has played only a very minor role to date. Here, it is important to create conditions that enable countermeasures to be taken. On the one hand, this includes strengthening training and further education opportunities that allow for specialization. Examples of this include dual training in the electronics industry, degree programs that also focus on new approaches in electronics development, and a much greater emphasis on practical applications in university teaching, for example through partnerships with companies for lecture series, internships, or guest lecturers.

Strengthen Skills & Workforce Development

"Build the workforce that builds the future: invest in chiplet and packaging talents."

"From schools to universities – secure the next generation of semiconductor experts."

However, the recruitment of skilled workers begins in schools and must be understood as a shared responsibility across society. STEM subjects need to be anchored far more firmly in school curricula, at least in Germany, supported by practical offerings for teachers and by STEM mentors who bring real-world industrial and business experience into the classroom. This effort should be complemented by political initiatives that actively promote a broad societal and entrepreneurial support culture, fostering early interest in technology and creating sustainable links between education, industry, and innovation ecosystems.

5. Glossary

ACP	Automotive Chiplet Program
ADK	Assembly Design Kit
AI	Artificial Intelligence
AIB	Advanced Interface Bus
AMA	Association for Sensors and Measurement
APECS	Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems
ASIC	Application-Specific Integrated Circuit
ASRA	Advanced SoC Research for Automotive
B2B	Business-to-Business
BoW	Bunch of Wires
CDX	Chiplet Design Exchange
CPU	Central Processing Unit
DARPA	Defense Advanced Research Projects Agency
DTCO	Design-Technology Co-Optimization
EDA	Electronic Design Automation
FMD	Forschungsfabrik Mikroelektronik Deutschland / Research Fab Microelectronics Germany
GPU	Graphics Processing Unit
GVC	Global Value Chain
HBM	High Bandwidth Memory
HIR	Heterogeneous Integration Roadmap
I3C	Improved Inter-Integrated Circuit
IC	Integrated Circuit
IDM	Integrated Device Manufacturer
IP	Intellectual Property
ISO 26262	Functional Safety Standard for Road Vehicles
JTAG	Joint Test Action Group
JU	Joint Undertaking
LCA	Life Cycle Assessment
MEMS	Micro-Electro-Mechanical Systems
NPU	Neural Processing Unit
OCP	Open Compute Project
OEM	Original Equipment Manufacturer
OSAT	Outsourced Semiconductor Assembly and Test
PCB	Printed Circuit Board
PDK	Process Design Kit
PMIC	Power Management Integrated Circuit
RF	Radio Frequency
RTO	Research and Technology Organization
SDV	Software-Defined Vehicle
SiP	System in Package
SME	Small and Medium-sized Enterprise
SoC	System on Chip
STEM	Science, Technology, Engineering, and Mathematics
STCO	System Technology Co-Optimization
TSV	Through-Silicon Via
UCIe	Universal Chiplet Interconnect Express
VDA	German Association of the Automotive Industry
VDMA	Machinery and Equipment Manufacturers Association
ZVEI	German Electro and Digital Industry Association

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